ABSTRACT OF THE DISCLOSURE

A counter for synthesizing clock signals with minimal jitter analyzes an ongoing count to determine whether the rising edge of an output clock should be triggered by the rising edge or falling edge of an input clock signal and to further determine whether the falling edge of the output clock should be triggered by the rising or the falling edge of the falling edge of the input clock signal. The counter may be implemented as a M/N:D counter in which a phase accumulator is compared to predetermined values to select the rising and falling edges of the output clock signal. In a default condition, the rising and falling edges of the output clock signal are triggered by rising edges of the input clock signal. However, if the accumulated phase value is greater than or equal to M/2 and less than M, an overriding signal will trigger the rising edge of the output clock based on the falling edge of the previous input clock cycle. If the accumulated phase value is greater than or equal to D+M/2 and less than M, the falling edge of the output clock is triggered by the falling edge of the preceding input clock signal. The use of rising and falling edges of the input clock signal reduces the jitter in the output clock signal and improves the duty cycle resolution. In addition, the clock circuit can produce a modulo-n signal with a 50% duty cycle. The designed architecture also produces an inverted output clock signal whose characteristics are identical to the non-inverted output clock signal (with the exception of duty cycle, which is inverted).